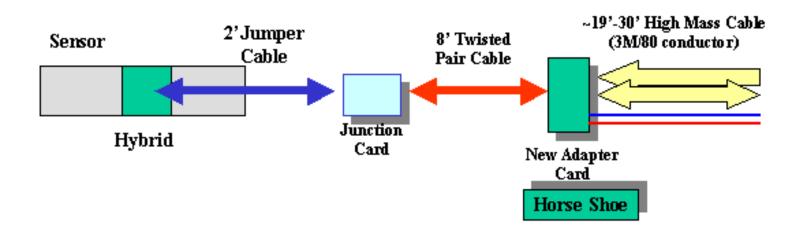


Electronics: Junction Cards, Adapter Card, Purple Card,

Ron Sidwell, K. Harder, T. Sobering, R. Taylor, E. VonToerne, *Kansas State U*.





Purple Card



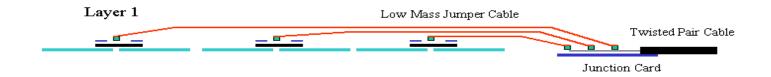
Communicates between
Standalone sequencer and hybrid.
50-conductor input cable, digital
jumper cable output. Voltage
regulation, signal translation,
temperature monitoring, etc., etc.

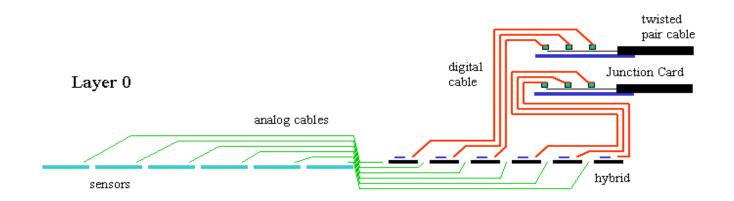
- Hybrid and module burnin and hybrid testing.
- Rev 2, twelve built. No design changes pending. But two failures of capacitor C42 recently-
- Do we need a readiness review before building final 75? Need 14-16 weeks for build and test.



Front-end Readout Cables

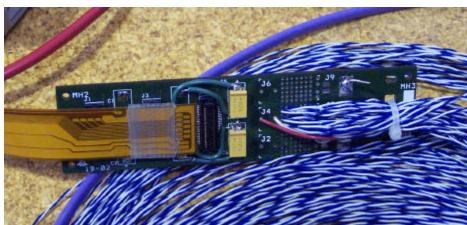








Junction Card



Joins twisted pair to digital jumper cable. Mounted at current position of H-disks.

- Only L1 has been prototyped. Request to enlarge solder pad area, more room for stubby fingers to solder in. No other pending design changes.
- Need to try 3 jumper cables! Do they fit?
- Need support drawing to understand constraints on size and mounting.
- Who is testing the assemblies? How many spares should we really build to allow for bad guys?

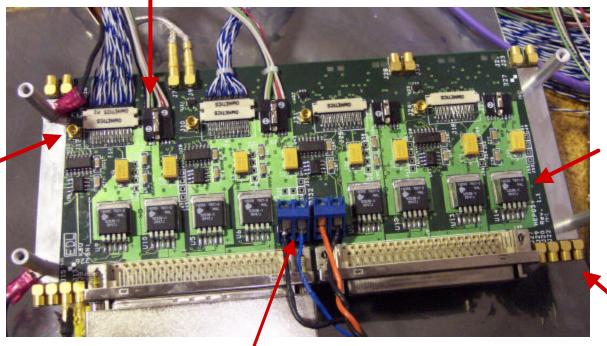


Adapter card

SVX4 power



CAL-SR(4)



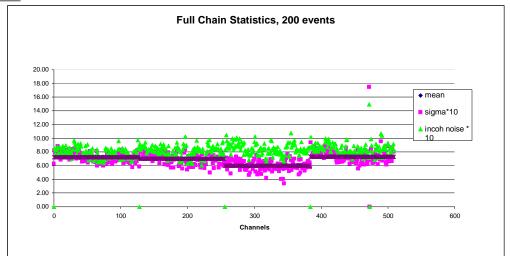
SVX4 Voltage regulators(8)

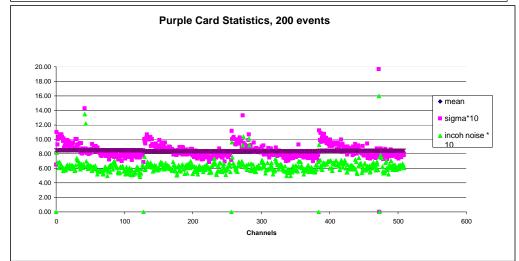
Clocks (16)

Board power



Full Chain vs Purple Card Readout



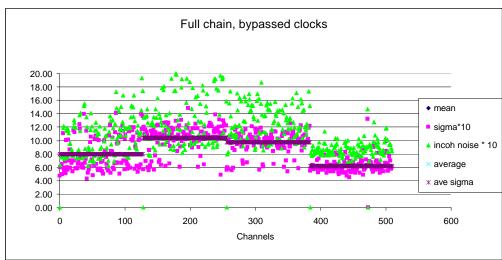


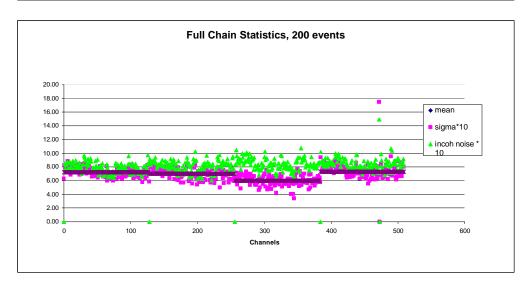
Pedestal not shown, just noise.

- Full chain, 200 events. No errors seen; but still can't run 10K events.
- Adapter card total noise level 0.1 adc counts lower. But incoherent higher. Need to investigate.



Can we bypass the clock?





• Use an old clock card from run2a to bypass the clocks (so they are not refreshed by the adapter card).

- Ouch.
- Still want to try union, when we can find some.

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Things to do

- Power, can we use one regulator, one power supply?
- Heat sinking. Measure del-T before and after with current setup.
- Size, shape of adapter card finalized.

- Termination of singleended lines (Utes, AN).
 Terminate on hybrid?
- Priority-in is too large (> 3V).
- Can we bypass clocks so that connectors and ICs can be removed from adapter card? Not promising so far.



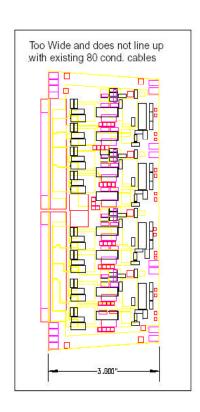
Needs before Rev 2 adapter card

- Heat sinking design
- Frozen layout (flat back edge)
- Clocks: yeah or nay?
- One vs two voltage regulators?
- Good communications (data corruption rate comparable to run 2a), and understanding of termination of single-ended lines.

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AC Change List (so far)





• Revised physical layout.

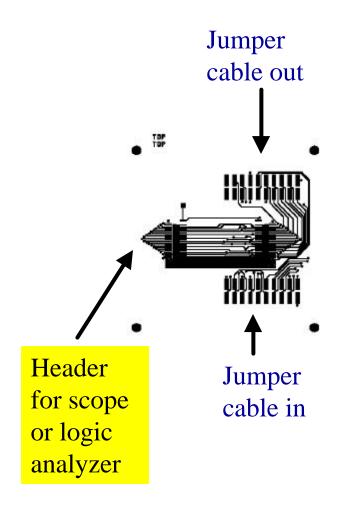
Other requests:

- Fuses for board power (3.3, 5v), and check limit on power traces. Input is 20AWG, 9A.
- Change power connector (4pin Vertical Molex)

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Russell's Breakout card (diagnostics)



- Allows one to spy on signals near, but not on, the hybrid (its safer that way).
- Should be ready in a week or two.



Interface Boards

- Interface board mods required so far for Run 2b:
 - 1. reprogram PLDs (in situ)
 - 2. modify clock voltage offset (change two resistors per channel, 16 per board)
 - 3. modify (or disable) current trip levels. I think they should remain but must be reset for more than 0.7 A. One-two resistors per channel.
 - 4. Cooper wants two analog temperature outputs per interface card. Design was for one. How do we do two?

What RTDs are to be used on the hybrids? IB expects 1000 ohm.



Comment on IB-SASEQ communication

- The standalone sequencer (SASEQ) has very different drivers and termination than the sequencer (12 vs 24 mA, 22 ohms series vs 80 ohm Thevenim equivalent.
- We had lousy communication unless we use the kludge (or buffer) card which plugs into the 50-conductor cable connector.
- Still can't run 10K events, maybe due to mechanical connector problems.

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